Resistive Switching Behavior Employing the *Ipomoea carnea* Plant for Biodegradable Rewritable Read-Only Memory Applications

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**ABSTRACT:** Development of biocompatible and biodegradable information storage could be one of the major strides toward the advancement of the next-generation eco-friendly electronics. Locally available leaves of *Ipomoea carnea* (IC) are employed to design a nonvolatile resistive memory device having the configuration Au/IC/ITO. The IC-based memory device is found to have back-to-back Schottky behavior. The memory device exhibits a very good ON/OFF ratio (~10^2), device yield (78%), reproducibility (≈32 cycles), and good physical stability (>360 days). Upon UV irradiation, the device performance improves in terms of a higher device yield (82%) and a larger memory window (10^3). Space charge-limited conduction, Schottky emission (SE), and metallic filament formation were the key behind the conduction mechanism for such observed switching behavior. Atomic force microscopy measurements have also been carried out in order to visualize the conduction filament in the IC-based resistive device. Temperature-dependent investigations confirmed that the gold filament and oxygen vacancy filament play an important role in the conduction mechanism. Based on the *I*−*V* characteristics as well as the data storage nature, it has been proposed that IC-based switching devices may be utilized to design rewritable read-only memory devices. This is an improvement of conventional write-once-read-many memory.

**KEYWORDS:** biodegradable, CAFM, nonvolatile, resistive memory, oxygen vacancy, rewritable read-only memory (RWROM)

1. **INTRODUCTION**

Nonvolatile memory technology has reached its limit in terms of scalability, high data density, fast switching speed, high power consumption, lower device size, and so forth.\(^1\)** In order to maintain the current pace of development in the field of electronic technology, emerging memories with distinctive advantages such as higher speed, high storage density, facile processing, and so forth are highly demanding.\(^3,4\) In this regard, the concept of memristor and resistive random access memory has emerged as a possible alternative to the existing memory technologies.\(^5−7\) Resistive switching (RS) has evolved with a great deal of scientific and technological advantages, fulfilling the demands of sustainable electronics toward the next-generation memory devices owing to its scalability, reliability, low power consumption, fast switching characteristics, compatibility in various substrates, inexpensive fabrication procedure, and so forth.\(^8,9\) RS refers to the physical phenomenon where a dielectric or insulator suddenly changes its resistance under the action of applied bias.\(^10−19\) In case of RS memory, typical memory-related figures of merit such as switching speed, data retention, ON/OFF ratio or memory window, integration density, endurance, and so forth are competitive with established conventional memory technologies.\(^20−22\) Moreover, generation of e-waste has become one of the burning issues due to the utilization of conventional Si-based memory devices.\(^23,24\) As per reports, India alone produces 52 million tons of e-waste which is 40% of the global share.\(^25\) Memory or data storage devices have contributed a large share to this e-waste. This is because, in the present big data era, the global data storage market size is projected to grow from USD 13.6 billion in 2022 to USD 38.5 billion by 2027 at a compound annual growth rate of 23%.\(^26\) Accordingly, the requirement for data storage devices has grown exponentially. Therefore, the biggest challenge to researchers is to find out alternative technology which is sustainable for the environment and at the same time that fulfills the demand of increasing data storage device requirements. In this regard, RS memory devices employing materials with biological origin as well as natural plant extract may play a crucial role.\(^27,28\) RS memory devices employing a wide range of biomaterials including proteins,\(^27,29\) carbohydrates,\(^23\) starch,\(^30\) biopolymers,\(^31,32\) cellulose,\(^33\) enzymes,\(^34\) pectins,\(^35\) glucose,\(^36\) and so forth have already been studied by different research
groups across the globe. On the other hand, there are few reports showing the use of natural plant materials toward realization of RS memory devices.\textsuperscript{37–39} Properties such as moderate to high charge carrier mobility, thermal stability across a wide temperature range, and high energy band gap make natural materials an attractive choice for the functional layer of electronic devices.\textsuperscript{40–42}

The main advantage of using natural materials is their environmental friendliness, biodegradability, and pollution-free as well as transient nature.\textsuperscript{43,44} In addition, there are several other advantages of natural material-based devices such as (i) the abundant accessibility of useful materials in our environment, resulting in a low cost of this memory device; (ii) such devices have amazing characteristics of self-decomposition that can be used for the application of security and military purpose; (iii) such devices are compatible with living systems, which makes them an ideal candidate to be implanted into the body of a living being without any hazardous effect. It has been shown that the implantation of bio-RRAM can be useful to study and even to control the behavior of animals.\textsuperscript{28}

The abundance of resources and simple low-cost device fabrication process of natural material-based electronic devices have opened up new gates to the advancement of the electronic world due to their applications as functional materials in various devices such as brain-inspired devices, sensors, wearable electronics, and so forth.\textsuperscript{30,45–47} Such advantages motivate us to further explore natural materials as functional layers in resistive memory devices. As far as the literature survey is concerned, very few natural materials such as aloe vera, apple, orange peel, and so forth have been reported to show RS.\textsuperscript{5,50}

Also, the exact mechanism lying behind the observed RS behavior in such devices is yet to be understood. On the other hand, stability of natural/biomaterial-based devices is a serious concern. Therefore, further investigation of natural plant-based RS devices is highly required. Also, a large number of plants need to be investigated.

Here, we report the RS behavior of a locally available plant Ipomoea carnea (IC)-based device. The extract of the IC plant consists of several organic compounds including carboxyl groups,\textsuperscript{51,52} which make it suitable for the electrical switching behavior. On the other hand, IC grows as a wild plant without any specific care and effort, making it easily available and the resulting device economic. At the same time, it is environmentally friendly and biodegradable. It has been observed that IC-based memory devices show back-to-back Schottky behavior. The IC-based device can be used to design nonvolatile memory devices with high data retention, endurance, cyclability, and a very good ON/OFF ratio (memory window). Interestingly, IC-based devices show very high physical stability with reproducible switching behavior even after 360 days. Based on the I–V characteristics, it has been demonstrated that the IC-based device is suitable for rewritable read-only memory (RWROM) application. This is an improvement of the conventional write-once-read-many (WORM) memory.\textsuperscript{53} In case of WORM, once the data is written, it cannot be erased but can be read again and again. However, in the present case, in addition to the existing WORM behavior, it is possible to reprogram the memory cell following a particular scan process. These results suggest the potential of the IC-based device toward the next generation of biodegradable nonvolatile memory device technology.

### 2. EXPERIMENTAL SECTION

#### 2.1. Preparation of the IC Active Solution

Leaves of IC were collected from the plant and washed with distilled water followed by complete drying of the same under shade at room temperature. Dried leaves were dissected into small pieces and pulverized by grinding them in a blender to enhance the effective contact with the solvent. The powdered material was again dried in a thermostatically controlled hot air oven below 45 °C until it attained a constant weight and passed through a 40-unit mesh sieve. A 12% ethanolic extract of the resulting dried powder of IC leaves was prepared by maceration. After waiting for 72 h, the content was centrifuged at 5000 rpm for 5 min. After centrifugation, only the supernatant part was used for device fabrication.

#### 2.2. Device Fabrication Process

For the electrical property measurement, a resistive memory device with configuration Au/IC/ITO was fabricated on an ITO-coated glass substrate. ITO was used as the bottom electrode and gold as the top electrode for all devices. In order to fabricate the device, the ethanolic extract of dried leaf powder of IC was deposited onto ITO-coated glass slides using the drop-casting method. The prepared device was then kept in a vacuum chamber for 24 h under ambient conditions. A shadow mask was used to deposit the gold electrode onto the IC film using the sputtering technique.

#### 2.3. Conducting Atomic Force Microscopy Imaging

The localized conduction paths of IC-based devices are investigated using a commercially available conducting atomic force microscope. These measurements were carried out using Park Scanning Probe System NXX10. In this measurement, a voltage was applied between the CAFM tip and ITO, where ITO acted as a bottom electrode. Details of the CAFM imaging have been reported elsewhere.

#### 2.4. FESEM Imaging

The surface morphology and cross-sectional view of an IC-based film were examined by a commercially available field effect scanning electron microscope (Sigma 300 model, Zeiss Pvt. Ltd.) operating at a 5 kV accelerating voltage. Energy-dispersive X-ray spectroscopy was used to examine the elemental composition of IC.

#### 2.5. I–V Characteristic Measurement

$I–V$ measurements of Au/IC/ITO were performed at room temperature using a Keithley 2401 SourceMeter. During the $I–V$ measurement, Au acts as the top electrode and ITO acts as the bottom electrode. Before the $I–V$ measurement, the prepared device was vacuum-dried out for at least 10 h. During the $I–V$ measurement, the step potential was 0.02 V. The schematic of the Au/IC/ITO device structure has been shown in Figure S1 of the Supporting Information.

### 3. RESULTS AND DISCUSSION

#### 3.1. Morphological Characterization

The surface and cross-sectional morphologies of the IC film and Au/IC/ITO device were investigated using FESEM. Corresponding images are shown in Figure 1a,b, respectively. The development of a smooth, nearly continuous IC layer onto ITO, is visible in Figure 1a. Figure 1b shows the thickness of the IC layer in the cross-sectional SEM image of the Au/IC/ITO/glass device, with a characteristic measurement.
where IC and ITO are easily distinguishable from one another. So, SEM studies give compelling visual evidence of smooth IC films of Au/IC/ITO devices.

### 3.2. Electrical Characterizations

Electrical characterization of the memory devices using IC as an active layer is demonstrated in Figure 2 under ambient conditions by applying suitable bias at the Au electrode while keeping ITO grounded.

Here, Figure 2a,b represents the linear and semilog current–voltage (I–V) curves of the Au/IC/ITO device measured in the optimal range of 0 to ±2 V with a compliance current (CC) of 5 mA. The device was scanned under DC bias in the direction 0 V → 2 V → 0 V → −2 V → 0 V at a rate of 0.02 V/step. The arrows in Figure 2 represent the scanning directions.

Upon scanning in direction 1, the device initially remained in the low-conducting high-resistance state (HRS), i.e., OFF state until the voltage reached 1.21 V, at which the current increased abruptly. Here, the device switched from the low-conducting HRS, i.e., OFF state, to the high-conducting low-resistance state (LRS), i.e., ON state. This is known as SET operation, and the corresponding threshold voltage is called SET voltage.\(^{54,55}\) The device maintained its LRS state while scanning direction 2, i.e., +2 V → 0 V. In the third scanning direction, i.e., 0 V → −2 V, the device exhibited switching behavior similar to that of the first scanning direction. Here, the device switched from its HRS to LRS at a negative threshold voltage of \(-1.05\) V and maintained this LRS in the fourth scanning direction from \(-2\) V → 0 V, like the second

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**Figure 2.** I–V characteristics of the Au/IC/ITO device: (a) linear scale and (b) semilog scale.

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**Figure 3.** (a) LRS and HRS behaviors of the device Au/IC/ITO for 32 switching cycles. Inset shows the corresponding I–V curves. (b) Plot of \(V_{SET1}\) and \(V_{SET2}\) of the Au/IC/ITO device for 32 switching cycles. (c) Read endurance measurement, 3600 times (one reading, 100 times). (d) Data retention characteristics of the Au/IC/ITO device measured for \(7 \times 10^4\) s.
scanning. The switching speed of the device was 100 ns. However, a significant behavioral change was observed between the $I−V$ characteristics during the positive (first) and negative (third) scan. During the third scan, initially, though the device was in an OFF state, it was conducting with a low magnitude of current which we termed as the HRS. On the other hand, during positive scanning, the device was in a completely OFF state initially. This may be due to the different conduction pathways during positive and negative scanning. Due to this, the two SET voltages were also different in the two scanning directions. This kind of RS behavior is described due to the switchable diode effect, indicating two back-to-back Schottky diode-like behaviors. The device was found to repeatedly change its state from the HRS to LRS in both scanning directions by changing the applied bias.

The memory window (ON/OFF ratio) is an important criterion from an application point of view. In order to have an idea about the memory window for the present device, we have calculated the memory window within the voltage range of 0.02−2 V at an interval of 0.02 V during the positive scan. The corresponding plot as a function of read voltage is shown in Figure S2 of the Supporting Information. It has been observed that in the read voltage range from 0.02 to 0.76 V, the memory window varies from $10^2$ to $10^3$. Beyond this range, the memory window is insignificant. In the present case, we have taken 0.2 V as the read voltage where the memory window is $1.02 \times 10^2$.

On the other hand, during the negative scan, the memory window is insignificant (Figure S3 of the Supporting Information). This indicates the existence of different conductive pathways in the two scanning directions. This has been discussed in light of different conducting pathways in the following sections.

The directional dependence of the RS property on the sweep direction was checked by reversing the initial scanning direction (0 V $→$ −2 V $→$ 0 V $→$ 2 V $→$ 0 V) (Figure S4 of the Supporting Information). In this case, the device also exhibits similar behaviors to those observed in the previous scanning directions with unaltered SET voltages. This proves

![Figure 4](https://example.com/fig4.png)

**Figure 4.** (a) Cumulative distribution of the operating set voltages in both positive and negative biases. (b) Stability of the Au/IC/ITO device for more than 360 days.

![Figure 5](https://example.com/fig5.png)

**Figure 5.** Fitted $I−V$ curves of the IC-based resistive memory device. Double-logarithmic plot for Au/IC/ITO in (a) positive bias and (b) negative bias. SE behavior for Au/IC/ITO in (c) positive bias and (d) negative bias.
the directional independence of the RS behavior of the Au/IC/ITO device in the initial scan direction.

In order to confirm the nonvolatile behavior of the current device, the device is switched to its ON state by applying a voltage sweep (0 → 2) followed by a reverse scan (2 → 0) which also shows low-resistance ON-state behavior (Figure S5 shown in the Supporting Information). The device is then completely disconnected from the power source. After some time, again, the power is turned on, and a voltage scan of 0 → 2 → 0 is applied. The corresponding I–V curve reveals that the device retains its ON state even after the removal of the external power supply (Figure S5 shown in the Supporting Information). This confirms that the present IC-based device shows nonvolatile memory behavior. 58,59

Information about the reproducibility and sustainability of the designed memory devices is required for probable practical and commercial applications. 53,60 Reproducibility of the designed memory device was checked in several consecutive scanning cycles in the direction 0 V → +2 V → 0 V → −2 V → 0 V (Figure 3a,b). Our investigations suggest that the device sustained its HRS and LRS without any significant degradation in the memory window (Figure 3a) and reproduced almost identical switching voltages ($V_{SET1}$ during positive bias and $V_{SET2}$ during negative bias) (Figure 3b) for at least 32 cycles. I–V curves for the 32 consecutive cycles are shown in the inset of Figure 3a. The results indicate good stability of the switching voltages and ON state corresponding to a single device for at least up to 32 consecutive cycles.

An idea about data endurance is also important for sustainable RWROM application of memory devices. Read endurance gives an idea about how many times the stored data can be read for a particular device. In this case, the LRS of the device was measured at an interval of 1 s at a read voltage of 0.2 V after switching the device to its ON state. At least 3600 times of read operation can be confirmed, maintaining the
memory window from the experimental results as shown in Figure 3c.

Investigation of the read retention property of a memory device provides information about how long the device can retain a particular state (HRS or LRS). Data retention property of the Au/IC/ITO device was checked by switching the device into the ON state, i.e., LRS, by applying a forward bias of 0 → 2 V and recording the LRS at a read voltage of 0.2 V as shown in Figure 3d. Observation of Figure 3d reveals that the device preserved the LRS for $7 \times 10^4$ sec, reported to be a better retention time for natural biodegradable materials as far as the literature survey is concerned. Therefore, our experimental observations reveal that the Au/IC/ITO device showed very stable, nonvolatile data retention and endurance properties for a considerable amount of time with negligible degradation in the memory window ($7 \times 10^4$ order), which is good enough for memory application. Here, it is important to mention that both endurance and retention properties were checked under positive bias only as under negative bias, the memory window was insignificant, potentially making the device less suitable for memory application with negative bias.

So, to improve the memory window and other switching parameters/properties, the effect of UV irradiation on the device was investigated as UV irradiation is known for generating defects in the active layer of the device that may change the conduction mechanism within the device, thereby changing the device performance. The effect of UV irradiation on the device performance is presented in detail in a later section.

Information about device yield is important to have an idea about device reproducibility. To check the device yield for Au/IC/ITO devices, I–V measurements were carried out for 42 independently fabricated almost identical switchable devices. Out of them, 33 devices showed reliable and reproducible switching behavior with a device yield of the order of 78.6%. The cumulative probability distribution of $V_{SET1}$ and $V_{SET2}$ in the positive and the negative scanning directions for all the devices is shown in Figure 4a with relative deviations of 12% for $V_{SET1}$ and 11% for $V_{SET2}$.

With the rapid development of science and the continuous progress of electronic technology, natural plant-based materials have become very promising for the next-generation memory application as a replacement for Si-based devices. Here, in our device, to check the long-term stability of Au/IC/ITO devices, I–V measurements were carried out with the passage of time. The observed results suggested reproducible and fairly reliable switching behavior even after 360 days from the day of device manufacture as shown in Figure 4b. As per the literature survey, physical stability of the order of greater than 360 days is advantageous for practical applications. Therefore, we expect that the designed device will show reliable memory behavior for an extended time duration.

To investigate the charge conduction mechanism of the Au/IC/ITO device, the I–V curves were plotted in the log–log scale for both positive and negative biases (Figure 5a,b) and linearly fitted to calculate the slope values for the selected voltage ranges. The linear fitting was done using "Origin 8.5" software. The I–V curves elucidate typical space charge-limited conduction (SCLC) behavior due to the charge transport phenomena in the IC active layer differentiated based on the values of the slope of different regions of log $I$–log $V$ curves. A slope value of 1 corresponds to Ohm’s law, whereas a slope value of 2 represents charge conduction based on electron-injected trap-controlled SCLC theory governed by Child’s law. On the other hand, for a slope value greater than 2,
charge conduction is reported to be due to the trap-filled SCLC theory; i.e., with the increase in voltage, the trap centers are occupied by charge carriers following Child’s law \((I \sim V^2)\) for charge conduction.\(^{2,3}\)

For both positive (Figure 5a) and negative biases (Figure 5b), the \(\log I-\log V\) plot of the IC-based memory device reveals the presence of four distinct regions \((R_1, R_2, R_3,\) and \(R_4)\), indicating that the conduction process in the IC active layer may be dominated by different conduction processes. In the \(R_1\) region, with a unity slope at the low bias of HRS, the \(I-V\) relationship is linear. This indicates that the charge conduction process obeys Ohm’s law in this region.\(^4\) Here, the charge conduction is dominated by thermally generated free charge carriers over the very small amount of injected carriers from the source electrode due to the application of very low bias voltage. With the increase in the applied bias, the slope of the \(I-V\) curve becomes almost 2 (1.77 for positive bias and 2.01 for negative bias) in the region \(R_2\). This suggests that the conduction process in this region is due to the injection of charge carriers from the source electrode. Here, the motion of the charge carrier is limited by trap centers pre-existing in the active layer. With the application of suitable bias voltage, these trap centers get filled up with charge carriers exhibiting a quadratic \(I-V\) relationship just after the ohmic region. This kind of charge transport behavior can be explained based on SCLC theory.\(^5,7,6\) The observed variation in the slope value is explained due to the depth of trap centers in the active layer.\(^7\) The trap center in the IC active layer may be formed due to the defects in the IC film or the chemical composition of IC.

In this regard, it is to be mentioned that IC leaves are reported to show the presence of 13 different kinds of compounds, some of which consist of the carboxyl group.\(^8\) Carboxyl groups are reported to be responsible to induce oxygen vacancies, thereby creating defects in the active layer.\(^9\) When the applied bias (both positive and negative biases) approaches \(V_{SET}\), almost all the traps are occupied by injected charge carriers, resulting in a sharp rise in the current with a slope much greater than 2, switching the device from the HRS to LRS (region \(R_3\)). Now, in the LRS, under both the biases during the reverse sweep, the device exhibited a linear \(I-V\) curve with a slope value nearly equal to 1 (0.99 for positive bias and 1.03 for negative bias), depicted as region \(R_4\), in Figure 5a,b. This indicates the probability of the formation of a conducting filament in the ON state following the ohmic \(I-V\) relationship.\(^10,8,1\)

The conduction mechanism of the Au/IC/ITO resistive device was further investigated by analyzing the \(I-V\) curves using standard theories. Figure 5c,d presents the fitting results of \(I-V\) curves under both positive and negative biases corresponding to the OFF (HRS) state of the device. Fitting results suggest a linear relationship of \(\ln I \sim V^{1/2}\) for both the biases in the high-voltage region with slopes of 6 for positive bias and 1.07 for negative bias. This suggests that charge carrier conduction in the HRS of the Au/IC/ITO device at low bias is due to \(SE\) under both biases.\(^2,8,2\)

To have a better understanding of the ON-state mechanism and to further check the possibility of filamentary conduction in the IC active layer of the RS device, \(I-V\) curves were analyzed at different temperatures ranging from 303 to 363 K. LRS resistance of the device was found to increase with increasing temperature during both the biases (Figure 6a,b), indicating the formation of metallic filaments.\(^83\) The memory window (ON/OFF ratio) of the device measured at different temperatures has been analyzed to have an idea about switching at different temperatures (inset of Figure 6a). A maximum memory window was observed for the device measured at 303 K. The observed high-memory window may be related to the higher chemical stability of the IC materials within the device, which gradually decreased with successive increases in temperature.

Linear fitting of the LRS resistances for both the bias directions was done using the equation \(R(T) = R_0 [1 + \alpha (T−T_0)]\), where \(R_0\) is the resistance of the device at temperature \(T_0\), \(\alpha\) is the temperature coefficient of resistance, and \(R(T)\) is the resistance at temperature \(T\). The determined value of \(\alpha\) for positive bias was found to be \(2.4 \times 10^{-3} \, \text{K}^{-1}\) and that for a negative bias was \(8.4 \times 10^{-1} \, \text{K}^{-1}\).

The order of values of \(\alpha\) is close to that of the gold filament (for positive bias) and oxygen vacancy-based filament (for negative bias).\(^85,86\) These results indicate that during positive bias, the Au filament was formed, and during negative bias, the oxygen vacancy-based filament was formed in the Au/IC/ITO device between the two electrodes to drive the device from the HRS to LRS.

To check the validation of the conductive filament formation in the aforementioned memory device under both positive and negative biases, CAFM measurements were done.\(^37,88\) CAFM is a widely used powerful technique to evaluate the existence of conducting channels. In this study, a gold (Au) CAFM tip was used as the top electrode and ITO as the bottom electrode. We have applied a \(\pm 2 \, \text{V}\) bias on an area of \(2.5 \times 2.5 \, \text{µm}^2\) in contact mode. The bias voltages were selected corresponding to the LRS of the device in both the bias directions. The experiment was performed at room temperature at atmospheric pressure without applying any current compliance. Spatially resolved current mapping images were obtained by moving the cantilever tip across the scanning area of the film surface. It has been observed that in positive bias (\(+2 \, \text{V}\)), a large number of conducting channels are formed (Figure 6c). On the other hand, in negative bias (\(-2 \, \text{V}\)), also a large number of conducting filaments can be seen (Figure 6d). Hence, we believe that the observed RS in the Au/IC/ITO device is due to conducting filament formation. However, a closer look at Figure 6c,d reveals that the two conducting channels formed during the two bias directions are different with respect to the distribution of current, shape, and size of the filaments. This clearly indicates that the conducting pathways in the IC active layer are different for two opposite bias directions. So, CAFM analysis along with the temperature-dependent resistance study clearly proves the formation of Au and oxygen vacancy filaments in the Au/IC/ITO device during the transition from the HRS to LRS in the positive and negative bias, respectively. This difference in the conduction channels during positive and negative scanning directions in the IC active layer is reflected in terms of different \(I-V\) characteristics (as observed in Figure 2) as well as memory windows. During positive bias (scanning direction 1 of Figure 2a), the device switches from the HRS to LRS due to the formation of the Au filament and maintains the LRS in scanning direction 2 (Figure 2a). During negative bias (scanning direction 3 of Figure 2a), instead of getting a linear \(I-V\) curve, we got a nonohmic semiconductor like the \(I-V\) curve, giving another set voltage. This is clearly due to a change in the conduction pathway during negative bias with respect to positive bias as discussed before. Here, the oxygen vacancy filament was formed during negative bias as evident...
from the temperature-dependent and CAFM study. This change in the conduction pathway may be responsible for different memory windows during positive and negative bias. From the above discussions, it is clear that the memory window depends on the conducting pathways inside the IC active layer. Again, it has already been discussed that IC active layer consists of pre-existing defects, mainly oxygen vacancy defects due to the presence of carboxyl groups as its active phytochemical constituents. Therefore, there is a probability to improve the memory window by changing the conduction pathways inside the IC active layer by varying the oxygen vacancy defect concentration in the active layer with the help of external stimuli. Improvement of the memory window is important for probable practical application.

3.3. Effect of UV Irradiation on RS Behavior. In many cases, it has been observed that external stimuli like UV irradiation affect the device performance with an increase in the memory window.\(^\text{67,69}\)

Accordingly, we have studied the effect of UV irradiation on the memory window and other device parameters of Au/IC/ITO. It has been observed that after 50 min of UV irradiation, the memory window increases up to 10\(^3\) compared to that of 10\(^2\) before UV irradiation during the initial positive sweep. However, during negative bias, the memory window remains insignificant even after UV irradiation. A similar result was reported by Shih et al. for UV irradiation of zinc oxide (ZnO)-based RRAM devices.\(^\text{66}\) From a practical application point of view, it is also important to check the effect of UV irradiation on other device parameters like reproducibility, sustainability, and device yield along with the memory window. The effect of UV treatment on these device parameters was checked by recording \(I-V\) data following the same measurement protocols as that before UV treatment in each case. Our investigations about the reproducibility of the device after UV irradiation suggest that the device sustained its HRS and LRS for 38 cycles, maintaining the memory window (∼10\(^3\)) (Figure 7a). This value is greater than that of a non-UV-irradiated device (32 cycles). Furthermore, fluctuations of current in the HRS and LRS of the non-UV-irradiated device (32 cycles) (Figure 3a) were stabilized to a considerable extent in the UV-irradiated device (38 cycles) (Figure 7a), thus improving the stability of the resistance states of the device. This shows that UV irradiation increases the reproducibility of the designed memory device. On the other hand, data retention analysis after UV irradiation showed that the device preserves its LRS for 5.04 × 10\(^4\) s (Figure 7b) compared to that of 7 × 10\(^4\) s for the non-UV-irradiated device. This indicates degradation in the data retention property with UV irradiation. Interestingly, it has been found that the device yield increases up to 82% after UV irradiation compared to the 78% for the non-UV-irradiated device. So, our experimental observations suggest that the Au/IC/ITO device with UV irradiation was more stable with better cyclability and device yield but with slightly low data retention properties for a considerable amount of time, maintaining a high memory window (∼10\(^3\)) than that of a non-UV-illuminated device. This is attributed to the higher production of oxygen defects obtained during UV illumination.\(^\text{67}\) The effect of UV irradiation on the characterization of the IC-based memory device was further investigated by calculating the cumulative probability distribution of \(V_{\text{SET1}}\) and \(V_{\text{SET2}}\) in positive and negative bias directions presented in the figure (Figure S6 of the Supporting Information). From this figure, it is observed that the relative deviation of both \(V_{\text{SET1}}\) and \(V_{\text{SET2}}\) decreased by a considerable amount after UV treatment of the device. Statistical cumulative distribution of switching voltages was taken for 38 consecutive switching cycles. So, the uniformity of the SET voltages in both the bias directions improved due to UV irradiation. Furthermore, it was observed that the SET voltage decreased to 0.96 V during the negative bias and increased to 1.37 V during the positive bias after UV irradiation. The corresponding \(I-V\) curves are shown in Figure S7 of the Supporting Information. These changes in the SET voltages are due to increased production of oxygen defects during UV treatment.\(^\text{67}\) After UV illumination due to the presence of a much higher concentration of oxygen defects with respect to the non-UV-illuminated device, migration of oxygen defects becomes easier under negative bias, thereby forming the oxygen vacancy filament at lower switching voltages. This explains the decrease in the SET voltage during negative bias. However, during positive bias, the switching is due to the formation of the gold filament both before and after UV irradiation. This was confirmed by calculating the temperature coefficient of resistance (\(\alpha\)) after UV illumination that matches the value obtained before UV illumination. After UV illumination, the presence of an excess amount of oxygen defects may offer some hindrance to the migration of gold ions from the top to the bottom electrode under positive bias, thereby increasing the SET voltage.

To further investigate the effect of UV irradiation on the stability and uniformity of the resistance states of the device, current distributions in terms of the cumulative distribution of the LRS and HRS for 38 consecutive switching cycles were measured. It has been found that relative distributions of current in the LRS and HRS have been decreased by 6 and 2% with respect to the non-UV-illuminated device shown in the inset of Figure 7a. This shows that the current in the LRS and HRS is more stable and uniform for UV-irradiated devices than for non-UV-irradiated devices.

3.4. Application as an RWROM Device. Here, we have mapped the RS behavior of Au/IC/ITO devices for non-volatile memory, especially WORM applications.\(^\text{53}\) In case of WORM memory, once the device is switched to a particular state, the device remains the same even though the bias is withdrawn. The corresponding state can be read again and again.\(^\text{53}\) Here, initially, the device is in the HRS. After the initial sweep, either at 0 → 2 V or 0 → −2 V, the device switched to its LRS (Figure 2). In both cases, the device maintains the LRS during reverse scan 2 V → 0 V or −2 V → −0 V. Under this condition, even if the bias is withdrawn, still, the device retains its LRS ON state and the same can be read again and again at a particular read voltage; in the present case, \(V_{\text{read}} = 0.2\) V. So, the information storage behavior is permanent in nature.\(^\text{53}\)

However, a close look at Figure 2 reveals that the device in the LRS (ON) state can be switched back to its HRS (OFF) state again by applying another particular scan cycle \(0\to 2\text{ V} \to 0\to −0.5\text{ V} \to 0\to −2\text{ V} \to 0\to 0.5\text{ V}\). This is confirmed by the follow-up scan from \(0\to 0.5\text{ V} \to 0\to −0.5\text{ V}\) (before the SET voltage; \(V_{\text{SET1}}\) or \(V_{\text{SET2}}\)) after the above scan. Thus, the device once again switched to the OFF state and was ready for another writing process. Now, the device can be switched to the LRS ON state once again by applying scan from \(0\to 2\text{ V} \to 0\to −2\text{ V}\). Consequently, the device holds this state. The corresponding state can be read multiple times. These results indicate that the present memory device based on IC as an active material can be used for...
RWROM applications. However, for a better memory window, the device should be operated with an initial positive scan (0 V → 2 V) rather than an initial negative scan (0 → −2 V) as the memory window is insignificant in the latter case.

3.5. Mechanism. The conduction mechanism for the formation of different kinds of conducting filaments during positive and negative bias is presented here. Under positive bias, the gold atoms near the interface of the gold top electrode and IC active layer get oxidized (Au → Au$^{+}$ + e$^{-}$) to gold ions (Au$^{+}$) and migrate toward the negatively biased ITO bottom electrode. Near the ITO bottom electrode due to the availability of injected electrons, Au$^{+}$ cations reduce to Au atoms (Au$^{+}$ + e$^{-}$ → Au) and deposit in the IC active layer near the bottom electrode interface. In this way, Au$^{+}$ cations reduce to Au atoms in the active layer and pile up to form a conductive bridge between the two electrodes under the influence of an increasing electric field driving the device into the LRS at a suitable SET voltage. Now, as evidenced by EDX analysis, the IC active layer may also contain several metallic ions like Na, Ca, Mg, and so forth (Figure S8 of the Supporting Information). These metallic ions may also participate along with Au atoms in the formation of a conductive bridge. However, the temperature treatment study proved the dominance of gold (Au) in filament formation.

During the reverse bias, the Au top electrode is negatively biased with respect to the ITO bottom electrode. As a result, electrons from the Au atoms present in the Au filament near the positively biased ITO electrode start to migrate toward the ITO electrode. Due to this stripping of electrons, the Au atoms present in the Au filament begin to oxidize (Au → Au$^{+}$ + e$^{-}$) and the resulting Au$^{+}$ ions migrate toward the negatively biased Au top electrode. As a result, the Au filament weakens significantly. However, a closer look at Figure 2b reveals that the current during the third scan (0 → −2) is higher compared to the OFF-state current during scan 1 (0 → 2). This suggests that the gold filament formed during scan 1 is not completely ruptured as soon as the negative bias is applied. However, with the prolongation of negative bias in the Au top electrode, all the atoms present in the Au filament are completely oxidized, resulting in the complete rupture of the Au filament. At the same time, negative bias injected electrons from the top electrode may charge and dislodge the negative oxygen ion from the metal oxides present in the IC active layer, leaving behind oxygen vacancy defect states and leading to the formation of a vacancy-mediated conduction bridge. As a result, the device again acquires a high-conducting state like that of scan 2.

The presence of metal oxides in the IC active layer is assumed to be due to the presence of different kinds of metals and oxygen present in the IC active layer as evidenced from the EDX analysis during SEM measurement. On the other hand, oxygen defects may also be formed due to the presence of different oxygen-containing functional groups such as the carboxyl group. In the present case, since the oxidation of Au atoms occurred at the Au/IC interface and created a large number of electrons, oxygen vacancy defect states were also created near the top electrode active layer interface. As a result of this vacancy creation, the active electrode further penetrates the IC active layer. This is because the oxygen vacancy is known to provide a local Fermi level close to the conduction band.

This increases the effective electric field inside the active layer between the electrodes, thereby accelerating the creation of further vacancy levels deeper into the IC active layer till the formation of a vacancy-mediated conduction bridge and once again driving the device from the HRS to LRS under the negative bias. There are literature reports regarding the formation of the metallic filament during positive bias and the oxygen vacancy filament during negative bias in the same device. Again, the temperature treatment study proved the formation of the oxygen vacancy filament during negative bias. Thus, the formation of oxygen vacancies conductive filaments may have competed with the rupture of the gold filament during negative bias, thereby forbidding the device to switch from the ON state to the OFF state.

Again, ITO can act as an oxygen reservoir due to its strong affinity for oxygen atoms. So, during the positive bias of the top electrode, all the oxygen anions were repelled by the negatively biased ITO bottom electrode toward the top electrode. During the migration through the active layer, oxygen anions may recombine with the oxygen vacancies pre-existing in the active layer. This explains the reason why in the present case only the Au filament is formed during positive bias. On the other hand, under the negative bias of the top electrode, ITO attracted all the oxygen anions, leaving behind the oxygen vacancies and resulting in the formation of an oxygen vacancy-based conducting filament. A schematic of the conduction mechanism during both positive as well as negative biases is shown in Figure 8.

In order to further investigate the mechanism of the effect of UV irradiation on the IC-based device, the $I$–$V$ curves were fitted with electrical conduction mechanisms. Figure 9a,b presents the fitting results of the $I$–$V$ curve of the UV-irradiated device under both positive and negative biases corresponding to the high voltage region of the HRS of the device. Interestingly, it has been observed that during positive bias, the $I$–$V$ curve obeys a linear relationship for $\ln(I/V)$ vs $V^{1/2}$, suggesting Poole–Frenkel conduction behavior (Figure 9a), which was SE-type before UV irradiation (Figure 5c). During negative bias, the conduction is SE-type (Figure 9b), the same as that before UV irradiation (Figure 5d). Thus, during positive bias, SE transformed into Poole–Frenkel, whereas during negative bias, there was no change. This transformation in the charge conduction mechanism of the OFF state may be due to the change in conduction pathways due to an increase in defects in the IC active layer induced by UV irradiation. The increase in the defect concentration in the active layer of the device would trap more electrons while positive bias is applied. This would decrease the OFF-state current (before SCLC). Furthermore, an increased number of defects would hinder Au$^{+}$ ion migration through the active layer and trapping of electrons would retard the reduction of Au$^{+}$ ions to Au atoms. This explains the increase in $V_{SET}$ during positive bias after UV treatment. However, once the Au filament was formed, the device switched to the LRS, maintaining almost the same ON state current as that before irradiation. So, the decrease in the OFF state current due to UV illumination resulted in an increase in the memory window ($I_{ON}/I_{OFF}$). However, there is no change in the memory window during negative bias. This may be due to the fact that conduction pathways remained the same before and after UV treatment both in LRS and HRS.

4. CONCLUSIONS

This paper presents a novel approach toward the development of a nonvolatile resistive memory device based on the configuration Au/IC/ITO with the RWROM application.
The RWROM application, which is a modification of the conventional WORM memory, improves the reliability and security of the device. The present memory device has an appreciable memory window (~10^6), reproducibility (more than 32 cycles), and a very high device yield (78%). The detailed analysis of the charge conduction mechanism was investigated based on the fitting of I−V curves, and it was found that SCLC, SE, as well as metallic filamentary conduction were the key mechanisms behind the observed I−V behavior. Temperature-dependent studies along with CAFM proved the formation of Au and oxygen vacancy filaments during positive and negative bias, respectively. After 50 min of UV irradiation, the concentration of oxygen vacancy increased, due to which the current conduction mechanism in the HRS transformed from Schottky to Poole−Frenkel during positive bias while remaining the same during negative bias. The change in charge conduction led to improvements in device parameters like a high ON/OFF ratio (~10^5), greater reproducibility (38 cycles), as well as device yield (82%). As a whole, our investigation revealed that IC-based RS devices may have very good potential for the realization of biocompatible sustainable electronics with a spatial emphasis on memory applications.

■ ASSOCIATED CONTENT

+ Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsaelm.3c00425.

Schematic representation of the device structure, variation of the memory window with different read voltages for positive bias, variation of the memory window with different read voltages for negative bias, current−voltage (I−V) behavior in the reverse direction of the device, nonvolatile behavior of the Au/Ipomoea Carnea/IITO device, cumulative distribution of SET voltages after UV irradiation, current−voltage (I−V) behavior after UV irradiation, and EDX images (PDF).

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Author Contributions

S.A.H. designed the work. F.Y.R. performed all experiments, F.Y.R., R.D., S.S., and H.B. analyzed the data. F.Y.R. and J.U. synthesized the material. S.A.H., F.Y.R., and S.C. wrote the manuscript with input from D.B.

Notes

The authors declare no competing financial interest.

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■ ABBREVIATIONS

RS, resistive switching; LRS, low-resistance state; HRS, high-resistance state; CAFM, conductive atomic force microscopy; SCLC, space charge-limited conduction; SE, Schottky emission; FESEM, field emission scanning electron microscopy; EDX, energy-dispersive X-ray spectroscopy; PE, Poole−Frenkel emission

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